



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,569	04/13/2004	Todd Kaplan	B-5327NP 621691-8	6558

7590 05/31/2005

Richard P. Berg, ESQ.
c/o LADAS & PARRY
Suite 2100
5670 Wilshire Boulevard
Los Angeles, CA 90036-5679

EXAMINER

NGUYEN, LINH V

ART UNIT	PAPER NUMBER
----------	--------------

2819

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/824,569

Applicant(s)

KAPLAN, TODD

Examiner

Linh V. Nguyen

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 April 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-67 and 69 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4-17, 20-33, 48-67 and 69 is/are allowed.
- 6) ☒ Claim(s) 2, 3, 18, 19, 34-36 and 41-47 is/are rejected.
- 7) ☒ Claim(s) 37-40 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. This office action is in response amendment filed on 4/11/05. Claims 2, 3, 4, 37 and 69 have been amended. Claims 1 and 68 have been canceled. Claims 2 – 67 and 69 are pending on this application.

Response to Arguments

2. Applicant's arguments filed 4/11/05 have been fully considered but they are not persuasive.

Under remarks, with respect to claim 34, applicant argued that "Adams does not teach a clock arrangement to pipeline the switch". Examiner respectfully disagrees from the following:

Fig. 6 of Adams discloses pipeline switches 22, 24 (transfer signal from one pipeline to another pipeline) with clock arrangement Clk 38 to pipeline (swap or no swap) the switch 22, 24 (also see fig. 8).

Under remarks, with respect to claim 41, applicant argued that "Adams does not teach a switch and a tuning arrangement to frequency adjust the switch". Examiner respectfully disagrees from the following:

Fig. 8 of Adams discloses switches 22, 24 and a tuning arrangement X3, X2, X1 to frequency adjusting (swap or not swap) the switches 22 or 24.

Under remarks, claim 2 have been considered but are moot in view of the same reference (Adams et al) from previous office action.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 2, 3, 18, 19, 34 - 36, and 41 - 47, are rejected under 35 U.S.C. 102(b) as being anticipated by Adams et al. U.S. Patent No. 5,404,142.

Regarding claim 2, Fig. 6 [20] of Adams et al. discloses switching arrangement (22, 24; Col. 4 lines 58 – 62) comprising: a digital input comprising a first digital input portion (A) and a second digital input portion (B); a digital output (Output of 20) comprising a first digital output portion (Out A) and second digital output portion (Out B); a switching element (22, 24) between the digital input (A, B) and the digital output (Out A, Out B), the switching element having a first condition (Col. 4 line 68 – Col. 5 line 2; disclosing “Low” condition of control signal 26) allowing the first digital output portion (Out A) to correspond to the first digital input portion (A) and the second digital output portion (Out B) to correspond to the second digital input portion (B) (Col. 4 line 64 – Col. 5 line 2), and a second condition (Col. 4 line 68 – Col. 5 line 2; disclosing “high” condition of switch control signal 26) allowing the first digital output portion (Out A) to correspond to the second digital input portion (B) and the second digital output portion (Out B) to correspond to the first digital input portion (A) (Col. 4 line 64 – Col. 5 line 2); and a control arrangement (30) to switch the switching element between the first

condition and the second condition (Col. 4 line 68 – Col. 5 line 2); a control arrangement (30) to switching (26) the switching element (20) between the first and second condition, wherein the control arrangement comprises analog processing elements (Col. 7 lines 58 – 61).

Regarding claim 3, wherein the control arrangement (30) has a first control input (IN A) connected with the first digital input portion (A), a second control input (IN B) connected with the second digital input portion (B), and a control output (26), the control output (26) allowing the switching element to assume the second condition (Col. 5 lines 31 – 34) if the first digital input portion is different from the second digital input portion (Col. 5 lines 44 – 46).

Regarding claim 18, wherein the switching element is a multiplexer (Fig. 6[20] disclosing multiplexing system for transmitting multiple signals A and B; See Webster Dictionary for “multiplex”).

Regarding claim 19, wherein the switching element is a latched multiplexer (Fig. 6[20] disclosing multiplexing system for transmitting multiple signals by using switches 24, 24 for engaging or latching the paths between input terminals [A, B] and output terminals [Out A, Out B]).

Regarding claim 34, Fig. 6 of Adams et al. discloses a circuit comprising: a first input (A) and a second input (B); a control element (30) connected with the first input and second input; a switch (20) either switching or not switching (Col. 4 line 64 – Col. 5 line 2) the first input (A) and the second input (B) according to the control element (30); and a clocking (Clk, 38) arrangement to pipeline the switch (Col. 5 lines 18 – 20).

Regarding claim 35, wherein the first input (A) and the second input (B) are digital inputs (Col. 8 lines 5 – 6).

Regarding claim 36, wherein the control element comprises a delta-sigma modulator (Col. 6 lines 3 – 5).

Regarding claim 41, Fig. 6 of Adams et al. disclose a circuit comprising: a first input (A) and a second input (B); a control element (30) connected (IN A, INB) with the first input (A) and the second input (B); a switch (20) either switching or not switching the first input and the second input according to the control element (Col. 4 line 68 – Col. 5 line 2); and a tuning arrangement (CountA – CountB) to frequency-adjust the switch (Col. 6 lines 51 – 55).

Regarding claim 42, wherein the first input (A) and the second input (B) are digital inputs (Col. 8 lines 5 – 6).

Regarding claim 43; wherein the control element comprises a delta-sigma modulator (Col. 6 lines 3 – 5).

Regarding claim 44, fig. 2 of Adams et al. further discloses wherein the delta-sigma modulator comprises a filtering element (capacitor array) and a quantizer (Quantizer).

Regarding claim 45, wherein the filtering element (capacitor array) comprises at least one delay element (every electrical device used to transfer signal is a delay element to its input signal).

Regarding claim 46, wherein the delay element comprises an adjustable gain circuit (the capacitor array is an adjustable gain circuit for the input signal).

Regarding claim 47, wherein the filter element (capacitor array) further comprises a plurality of transconductors (capacitor is a electrical conducting element use to transfer signal) , and wherein the turning arrangement frequency (switching circuit of Fig. 6) adjusting at least one transcoductor of the plurality of transconductors.

Allowable Subject Matter

5. Claims 37 - 40, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. With respect to claim 37, in addition to other elements in the claim, the prior art does not teach wherein the clocking arrangement clocks the filter element and the quantizer.

6. Claims 4 – 17, 20 - 33, 48 – 52, and 53 – 67, and 69 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claim 4, in addition to other elements in the claim, the prior art does not teach wherein the control arrangement comprises a subtractor, subtracting the first digital input portion from the second digital input portion, the subtractor having a subtractor output with a first subtractor output value if the first digital input portion is not in a predetermined relationship with the second digital input portion and a second subtractor output value if the first digital input portion is in a predetermined relationship with the second digital input portion.

With respect to claims 48 and 53, in addition to other elements in the respective claim, the prior art does not teach a control element to control switching of the switch,

the control element connected with the evaluation element and the switching element, the control element comprising a quantizer having a quantizer output, wherein switching between the first digital input and the second digital input depends on the quantizer output when the first digital input and the second digital input are in predetermined relationship therebetween and switching between the first digital input and the second digital input does not depend on the quantizer output when the first digital input and the second digital input are not in the predetermined relationship therebetween.

With respect to claim 69, the prior art does not teach a first DAC having a first DAC input and a first DAC output; providing a second DAC having a second DAC input and a second DAC output; connecting the first circuit output with the first DAC input and the second circuit output with the second DAC input; subtracting the second DAC output from the first DAC output to provide a difference output; and inputting the difference output to a spectrum analyzer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

5/18/05

Linh Van Nguyen

Art Unit 2819


Michael Tokar
Supervisory Patent Examiner
Technology Center 2800